REMARKS

Claims 6, 7, 9, 11-13 and 15-19 are pending in the present application. Claims 6, 11, and 16 have been amended. Claim 8 has been canceled.

Information Disclosure Statement

Applicant acknowledges receipt of the signed and dated Information Disclosure Citation Form PTO-A820 along with the current Office Action dated December 21, 2005. References A through D have lines there through, indicative that the citations are not in conformance and not considered.

Applicant also acknowledges receipt of another signed and dated copy of the same Information Disclosure Information Disclosure Citation Form PTO-A820 along with the Office Action dated July 31, 2002. Each of references A through D have been initialed by the Examiner, indicative that the references have been considered and will be cited of record.

In view of this inconsistency, the Examiner is respectfully requested to confirm on the record that the references listed in the Information Disclosure Statement filed along with the present divisional application on January 25, 2001, have been considered and will be cited of record in the present application.

Claim Rejections-35 U.S.C. 112

Claims 6-9 and 11-19 have been rejected under 35 U.S.C. 112, first paragraph,

as failing to comply with the written description requirement. The Examiner has asserted that the specification does not reasonably convey that the inventor had possession of the claimed invention, wherein the sidewall spacers of silicon oxide film are "not on the side surfaces of said protective layer", as featured in claims 1, 11 and 16.

However, the above noted features have been deleted from the independent claims. Claims 6, 7, 9, 11-13 and 16-19 should thus be in compliance with 35 U.S.C 112, first paragraph. The Examiner is therefore respectfully requested to withdraw this rejection for at least these reasons.

Claims 6-9 and 11-19 have been rejected under 35 U.S.C. 112, second paragraph, as being indefinite. The Examiner has asserted that the features whereby the sidewall spacers are "not on the side surfaces of said protective layer", are negative limitations that render the claims indefinite. Although Applicant does not necessarily concede that this rejection is proper, these features have been deleted from the independent claims as noted above, merely to advance prosecution of this application. Claims 6, 7, 9, 11-13 and 16-19 should thus be in compliance with 35 U.S.C 112, second paragraph. Accordingly, the Examiner is respectfully requested to withdraw this rejection for at least these reasons.

Also, claim 16 has been amended to feature that the sidewall spacers of silicon oxide film are formed on side surfaces of the gate. Claim 16 should thus be in compliance with 35 U.S.C. 112, second paragraph.

Claim Rejections-35 U.S.C. 102

Claims 16-19 have been rejected under 35 U.S.C. 102(b) as being anticipated by the Yoo et al. reference (U.S. Patent No. 5,605,853). This rejection, insofar as it may pertain to the presently pending claims, is traversed for the following reasons.

The semiconductor device of claim 16 includes in combination a gate; a field oxide; a protective layer "formed directly on said field oxide to prevent overetching of said field oxide, said protective layer being a conductive layer, having side surfaces thereof over said field oxide, and having substantially uniform thickness"; sidewall spacers; and an insulating layer. Applicant respectfully submits that the Yoo et al. reference does not disclose these features.

As noted above, the protective layer of claim 16 is formed directly on the field oxide and has substantially uniform thickness. As described beginning on page 11, line 18 of the present application with respect to Fig. 1(e), a chemical mechanical polishing (CMP) is used to flatten a rugged portion of the surface, whereby silicon nitride layer 33 is used as a CMP stop. Accordingly, polysilicon layer 12 after CMP processing would inherently have substantially uniform thickness. This advantageously reduces the occurrence of steps on the field oxide layer.

The Examiner has interpreted floating gate 21 in Fig. 7 of the Yoo et al. reference as the protective layer of claim 16. However, as described beginning in column 3, line 64 of the Yoo et al. reference, a first layer of polycrystalline silicon is deposited, and the polysilicon is patterned by conventional lithography and etching to

form gate electrodes 16, polysilicon interconnects 16' and floating gate 21. Since floating gate 21 of the Yoo et al. reference is formed by conventional lithography and etching, floating gate 21 does not have substantially uniform thickness, and thus cannot be interpreted as the protective layer of claim 16. Applicant therefore respectfully submits that the semiconductor device of claim 16 distinguishes over the Yoo et al. reference as relied upon by the Examiner, and that this rejection, insofar as it may pertain to claims 16-19, is improper for at least these reasons.

Claim Rejections-35 U.S.C. 103

Claims 6-9, 11-13 and 15 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Watabe reference (U.S. Patent No. 5,525,530), in view of the Amakawa reference (Japanese Patent Publication No. 2-257637). This rejection, insofar as it may pertain to the presently pending claims, is traversed for the following reasons.

The semiconductor device of claim 6 includes in combination first and second gates; a field oxide; a protective layer "formed directly on said field oxide to prevent overetching of said field oxide, said protective layer being a conductive layer, having side surfaces thereof over said field oxide, and having substantially uniform thickness"; sidewall spacers of silicon oxide; and an insulating layer. Applicant respectfully submits that the prior art as relied upon by the Examiner does not make obvious these features.

The Examiner has primarily relied upon the Watabe reference as showing all the

features of the claim, except for the protective layer formed on the field oxide. In an effort to overcome this acknowledged deficiency, the Examiner has asserted that the Amakawa reference teaches a polysilicon protective layer film 7 as shown in Fig. 1(e).

However, as described in the English translation of the Amakawa reference, second polysilicon film 7 is etched, and thus does not have substantially uniform thickness, as may be clearly understood in view of Fig. 1(e). Second polysilicon film 7 of the Amakawa reference thus cannot be interpreted as a protective layer of claim 6. Applicant therefore respectfully submits that the semiconductor device of claim 6 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection, insofar as it may pertain to claims 6, 7 and 9, is improper for at least these reasons.

The semiconductor device of claim 11 includes in combination a gate; a field oxide; a protective layer "formed directly on said field oxide to prevent overetching of said field oxide, said protective layer being a conductive layer, having side surfaces thereof over said field oxide, and having substantially uniform thickness"; sidewall spacers; and an insulating layer.

As emphasized above with respect to claim 11, second polysilicon film 7 of the Amakawa reference cannot be interpreted as the protective layer of claim 11. Applicant therefore respectfully submits that the semiconductor device of claim 11 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection, insofar as it may pertain to claims 11-13 and 15, is

improper for at least these reasons.

Conclusion

The Examiner is respectfully requested to reconsider and withdraw the corresponding rejections, and to pass the claims of the present application to issue, for at least the above reasons.

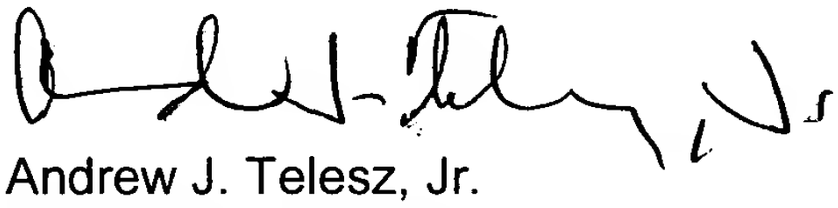
In the event that there are any outstanding matters remaining in the present application, please contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (571) 283-0720 in the Washington, D.C. area, to discuss these matters.

Pursuant to the provisions of 37 C.F.R. 1.17 and 1.136(a), the Applicant hereby petitions for an extension of one (1) month to April 21, 2006, for the period in which to file a response to the outstanding Office Action. The required fee of $120.00 should be charged to Deposit Account No. 50-0238.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment for any additional fees that may be required, or credit any overpayment, to Deposit Account No. 50-0238.

Respectfully submitted,

VOLENTINE FRANCOS & WHITT, P.L.L.C.



Andrew J. Telesz, Jr.
Registration No. 33,581

One Freedom Square
11951 Freedom Drive, Suite 1260
Reston, Virginia 20190
Telephone No.: (571) 283-0720
Facsimile No.: (571) 283-0740